a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads.

REMARKS

Claim 13 has been rewritten in independent form. Since this claim was previously indicated to contain allowable subject matter, it is presumed that the claim is in allowable form.

In the outstanding office action claims 14-17 were rejected as being anticipated by Yamaguchi. This rejection is respectfully traversed. Specifically, these claims all depend directly or indirectly from claim 13 and therefore are believed to be allowable for at least the reasons that claim 13 is allowable. They are also believed to recite additional features that when considered in the context of the claimed invention, further patentably distinguish the invention from the art of record.

Claim 11 has been amended to better define the panel based feature that was one of the aspects that claim 14 originally sought to articulate. It is believed that with this amendment, the presently presented claims are clearly patentable over the art of record. It is noted that Applicant expects to file a continuation directed at other features of the invention and reserves the right to introduce additional claims that better define these and other patentable features of the invention.

The Yamaguchi Reference.

It is acknowledged that Yamaguchi discloses a surface mount package having a lead frame with exposed planar contacts and a planar die attach pad (see, e.g., Figs. 3A and 3B). However claim 11, as amended, specifically requires a lead frame panel that has a molded cap that covers an array of devices. Such a structure has significant manufacturing advantages over the lead frame strips described by Yamaguchi. For example, as is apparent from the

specification, when a plastic encapsulating "cap" can be molded over a lead frame panel having an array of separate device areas, a relatively inexpensive mold can be used to encapsulate a relatively larger number of devices. Each surface mount package can then be formed merely by singulating the individual devices (e.g., by sawing). In contrast, Yamaguchi, discloses a lead frame panel (which takes the form of a strip) that individually encapsulates each device. [Of course, each of the devices on the lead frame strip may be molded at the same time, but they are still individually molded]. This is best illustrated in Fig. 6(c) and is described at Col. 5, lines 27-41. Group molding as also permits the devices to be positioned more closely together than would be possible in individually encapsulated devices such as described by Yamaguchi. It should be apparent that individually molding each device is a significantly more expensive process than the array base molding approach disclosed in the specification.

It is appreciated that claim 11 (like original claim 14) is not directed at the method of manufacturing the semiconductor package. Rather, as amended, claim 11 is directed at the panel structure itself. The claimed panel structure can be used to produce packages in a significantly easier manner than the panel structures disclosed by Yamaguchi. Therefore, it is respectfully submitted that the presently claimed structure is neither anticipated nor obvious in view of the Yamaguchi reference (or any of the other art of record)

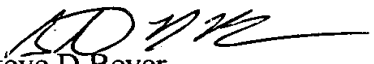
The Aono Reference.

Like Yamaguchi, Aono discloses a surface mount package having a lead frame with exposed planar contacts and a planar die attach pad (see, e.g., Figs. 2A, 2B, 8A and 8B). However the package structure disclosed by Aono has leads that extend beyond the encapsulation. Although such extended leads have certain benefits, they inherently require that each device be **individually molded**. Accordingly, it is respectfully submitted that Aono has the same drawbacks as discussed above with respect to Yamaguchi.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance. If the examiner has any remaining concerns about the application, he is respectfully requested to contact the undersigned at the number set forth below.

If any fees are due in connection with the filing this Response, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P217D2).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Steve D Beyer
Registration No. 31,234

P.O. Box 778
Berkeley, CA 94704-0778
(ph.) (650) 961-8300

MARKED UP VERSION OF THE CLAIMS INDICATING THE CHANGES MADE

11. (Twice Amended) A[n] lead frame panel suitable for forming an array of integrated circuit packages for accommodating a semiconductor die, the lead frame panel having an array of device areas, each device area being suitable for forming an independent integrated circuit package and comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads [having] has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads, wherein the plastic encapsulation is part of a molded cap that covers an array of the device areas.

13. (Amended) An integrated circuit package [as recited in claim 11,] for accommodating a semiconductor die, [further] comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said

upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads.